REMARKS

The Examiner's Office Action of February 8, 2005 has been received and its contents reviewed. Applicant would like to thank the Examiner for the consideration given to the above-identified application, for indicating the allowance of claims 17-20, and for indicating claim 24 as containing allowable subject matter and would be allowable if rewritten in independent form.

By this Amendment, claims 1, 5, 9, 13 and 21 have been amended. Accordingly, claims 1-25 are pending for consideration, of which claims 1, 5, 9, 13, 17 and 21 are independent. By the actions above and the remarks below, Applicant respectfully requests reconsideration and allowance of all the pending claims.

Referring now to the detailed Office Action, claims 1, 2 and 4 stand rejected under 35 U.S.C. §102(b) as anticipated by Borel et al. (U.S. Patent No. 6,297,093 B1 – hereinafter Borel). Further, claims 3 and 5-8 stand rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Murai (U.S. Patent No. 5,473,184 – hereafter Murai). Still further, claims 9, 10 and 12 stand rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Papadas et al. (U.S. Patent No. 5,687,113; hereinafter – Papadas). Still further, claim 11 stands rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Papadas and further in view of Murai. Still further, claims 13-16 stand rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Murai and Papadas. Finally, claims 21-23 and 25 stand rejected under 35 U.S.C. §103(a) as unpatentable over Liang (U.S. Patent No. 6,180,502 B1) in view of Papadas. Each of these rejections is traversed for the reasons advanced in detail below.

With respect to the §102(b) rejection of claims 1, 2 and 4 of Borel, Applicant has amended independent claim 1 to replace "a substrate" with "insulating surface", as shown above, to further clarify the claim language and to distinguish over the cited prior art reference. The presently claimed invention solves a problem wherein a semiconductor device is prone to be charged and damaged by plasma during anisotropic etching to form sidewalls, as disclosed in page 3, lines 24-26 of the specification. Applicant respectfully asserts that the rejection based on Borel, which does not disclose using insulating material, over which a semiconductor film would be formed, is inappropriate. That is, Borel fails to disclose forming a semiconductor film over an insulating surface, as recited in amended claim 1.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Borel, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1, 2 and 4 as anticipated by Borel is improper.

The Examiner asserted that Borel discloses the device that is to be incorporated with CMOS structure manufacturing, therefore, the device will inherently incorporate a logic circuit. However, Applicant respectfully asserts that a device with CMOS structure is widely used and not limited to a logic circuit. Applicant respectfully requests the Examiner to further explain the assertion and how it is applicable in this rejection.

With respect to the §103(a) rejection of claims 3 and 5 over Borel in view of Murai, particularly with respect to claim 3, the Examiner asserts that an impurity is added through two layers 2 and 5 of Murai. However, the layers 2 and 5 of Murai are a gate oxide film and a silicon dioxide film, respectively, as disclosed in column 3, lines 21 and 38 of Murai, and not conductive film as alleged by the Examiner.

With respect to independent claim 5, Applicant has amended the claim in similar manner as claim 1. The arguments set forth above in relation to the §102(b) rejection are also applicable.

With respect to the §103(a) rejection of claims 9, 10 and 12 over Borel in view of Papadas, Applicant have amended independent claim 9 similarly as claim 1. The spacers (i.e., "sidewalls") 28 and 29 of Papadas are formed using conductive material, as disclosed in column 6, lines 38-41 of Papadas. Therefore, the element of Papadas would not be charged and damaged by plasma during process of forming spacers (i.e., "sidewalls"). As a result, the combination of Papadas with Borel is improper without proper motivation or suggestion in Papadas to use a non-conductive material as spacers.

With respect to §103(a) rejection of claims 13-16 over Borel in view of Murai and Papadas, Applicant has amended independent claim 13 in a manner similar to claim 1. Applicant respectfully asserts that the rejection should be withdrawn because independent claim 13 is essentially a combination of all the features of claims 5 and 9.

With respect to the §103(a) rejection of claims 21-23 and 25 over Liang, in view of Papadas, Applicant has amended independent claim 21 to add a feature of a sidewall being formed over the conductive film, as shown above. Since the sidewalls of Liang and Papadas is not formed over the conductive film, as disclosed in FIG. 27 of Liang and Fig. 3C of

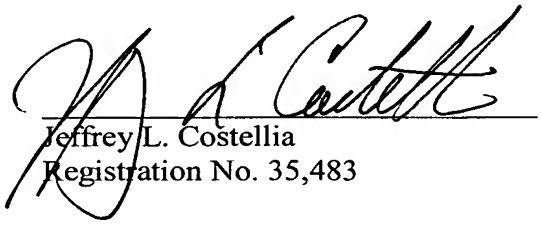
Papadas, Applicant respectfully asserts that the amendment clearly and sufficiently distinguishes over the cited prior art references.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Liang and Papadas fail to teach, disclose or suggest forming a sidewall over the conductive film to a side surface of the gate electrode wherein the gate insulating film being covered by the conductive film, their application in the §103(a) rejection is improper.

In view of the amendments and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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